JITTER REDUCTION

[ABSTRACT OF THE DISCLOSURE]

Digital circuitry, for use for example in a mixed-signal device such as a digital-to-analog converter, has decoders (22, 24) which process a digital input word (D1~Dm) to derive thermometer-coded signals (T, $\bar{T}$) for controlling one cell of an array of cells in the device. The decoders commence operation at the rising edge of a first clock signal (DIGCLK). Each cell has a first, D-type latch (26) clocked by a second clock signal (CLK2) that is delayed by a preselected delay time Δ_1 relative to the first clock signal, and a second, transparent latch (32) clocked by a third clock signal (CLK3) whose rising edge coincides with the rising edge of the first clock signal and whose falling edge coincides with the rising edge of the second clock signal. The rising edge of the third clock signal is not affected by jitter associated with a delay element (28) used to delay the first clock signal by Δ_1. The falling edge is affected by such jitter, so outputs (TCK, $\overline{TCK}$) of the first latch have jitter at the falling edge, but this is prevented from feeding through to final outputs (TS, $\overline{TS}$) of the circuitry because the second latch is non-transparent at that falling edge.

[Fig. 6]